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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,865	12/05/2003	En-Hsing Chen	023-0029	8494

52100 7590 09/12/2007
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ART UNIT	**PAPER NUMBER**
2824	

MAIL DATE	DELIVERY MODE
09/12/2007	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/729,865
Filing Date: December 05, 2003
Appellant(s): CHEN ET AL.

Andrew C. Graham
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 06/05/2007 appealing from the office action mailed 07/28/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The amendment after final rejection filed on 11/28/2006 has been entered.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,380,636	TATSUKAWA	4-2002
6,411,548	SAKUI et al.	6-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,380,636 Tatsukawa (hereinafter "Tatsukawa").

Regarding claim 1, Tatsukawa discloses an integrated circuit comprising a memory array (memory cell array MA, see FIG. 7) including memory cells arranged in a plurality of series-connected NAND strings (see FIG. 8), said memory cells comprising modifiable conductance switch devices (floating gate memory cells MC11-MC22, which are programmed by tunneling current), said NAND strings including at a first end thereof a respective plurality of series selection devices of like type (select transistors DG1 and SGD1 connected to the first end of the NAND string on the left, select transistors SGS2 and DG4 connected to the first end of the NAND string on the right, see FIG. 8), wherein each NAND string includes a second plurality of series selection devices of like type at a second end thereof (select transistors SGS1 and DG2 connected to the second end of the NAND string on the left, select transistors DG3 and SGS2 connected to the second end of the NAND string on the right, also see FIG. 8), and wherein pairs of NAND strings are arranged so that (pair of NAND strings shown in FIG. 8):

a first group of control signals couples to the respective second end of one string of the pair to a global array line associated with the pair, and couples the respective first end of the other string of the pair to a respective bias node (control signals SS1 and SD2 connecting NAND string on the right to the main bit line MBL, and NAND string on the left to a program inhibit voltage); and

a second group of control signals couples the respective first end of said one string of the pair to a respective bias node, and couples the respective second end of the other string of the pair to the global array line associated with the pair (control signals SS2 and SD1 connecting NAND string on the left to the main bit line MBL, and NAND string on the right to a program inhibit voltage).

(See column 13, line 17 to column 14, line 18)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tatsukawa in view of U.S. Patent No. 6,411,548 to Sakui et al. (hereinafter "Sakui").

Tatsukawa discloses, as applied in prior rejection of claim 1, all claimed subject matter except further limitations as set forth in claims 27-28.

Regarding claim 27, Sakui also discloses series selection devices having a charge storage dielectric (select gate transistors S1(s) having block insulating films 40SSL between the control gate 27SSL and charge storing layer 26SSL, see FIG. 44).

Since Tatsukawa and Sakui are both from the same field of endeavor, the purpose disclosed by Sakui would have been recognized in the pertinent art of Tatsukawa.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to implement the structure of select gate transistors substantially the same as that of each memory cells for the purpose of reducing the area of the chip and the manufacturing cost (see column 39, line 55 to column 40, line 6).

Regarding claim 28, Sakui further discloses series selection devices are maintained by periodic programming biasing to a higher threshold voltage than fabricated (see FIGS. 52-53).

(10) Response to Argument

(I) **Ground I**: The rejection of claim 1 under U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,380,636 to Tatsukawa (hereinafter "Tatsukawa").

Claim 1

(I-a) Appellant argues that, as shown in Tatsukawa, FIG. 8, only transistor SGS1 corresponds to a selection device at this end of this NAND string because the connection to the source line SL1 is made just "beyond" transistor SGS1, as viewed from the perspective of the NAND string. Specifically, the common node between transistors SGS1 and DG2 is itself the source line SL1. In other words, Appellant argues that transistor DG2 does not correspond to a

selection device at the end of the NAND string because the connection to the source line SL1 is not made just "beyond" DG2 (see Appeal Brief page 4, paragraph 1).

In response to (I-a), Tatsukawa clearly shows DG2 is connected in series with SGS1, both DG2 and SGS1 are connected to the NAND string, and both DG2 and SGS1 are connected to the second end of the NAND string (see Fig. 8). Therefore, DG2 corresponds to a selection device at an end of the NAND string.

Further, Examiner submits that claim 1 does not specifically recite where the second end of the one NAND string exists with respect to the second selection devices. In other words, there is no specific connectional relationship recited in claim 1 between the second end and the second selection-devices, other than the second selection devices are simply "*include[d]... at a second end.*" Thus, Examiner submits that Appellant's arguments are based upon limitations which are not recited in claim 1 in order to distinguish the claim over Tatsukawa.

However, even assuming arguendo that this unrecited limitation is inherent in claim 1, which it is not, then Examiner submits the following to rebut Appellant's argument.

Appellant's attention is directed to FIG. 8 of Tatsukawa, and column 14 lines 14-18, to wit:

> "Sub-bit lines SBL1 and SBL2 as well as *the sub-source lines in the structure shown in FIG. 8 are formed by regions where the source/drain impurity diffusion layers of the memory cell transistors continue to the impurity diffusion layers of the block select transistors.*" (Emphasis added)

And also to FIG. 5 of Tatsukawa, column 10 lines 46-56, where DG2 is described in the context of different memory cell arrangement than FIG. 8, to wit:

> "Conductive layers 5-1, 6-1 and 4-2 extend in the row direction, and cross impurity regions 2-1a and 2-2a. Conductive layer 5-1 transmits source-side block select signal SS1, conductive layer 6-1 forms source line SL1, and conductive layer 4-2 transmits drain-side block select signal SD2. In regions where conductive layers 4-2 crosses impurity regions 2-1a and 2-2a, source-side block select transistor SGS1 and dummy transistor DG3 are formed, respectively. *Likewise, dummy transistor DG2 and drain-side block select transistor SGD2 are formed in regions where conductive layer 4-2 crosses impurity regions 2-1a and 2-2a.*" (Emphasis added)

A NAND string often comprises a series of memory cells and select transistors connected between a sub-bit line and a sub-source line. From the above paragraphs, the sub-source line of the NAND string corresponding to sub-bit line SBL1 shown in FIG. 8 is formed by impurity diffusion layer/impurity region, where dummy transistor DG2 is defined.

Tatsukawa still shows DG2 is connected in series with SGS1, both DG2 and SGS1 are connected to the NAND string, and both DG2 and SGS1 are connected to the second end of the NAND string.

(I-b) Appellant argues that dummy transistor DG2 *cannot be seen as a select device* because a select device within, and at one end of, a NAND string functions to couple a series connected string of memory cells within the NAND string to some kind of memory array node (e.g., global array line, main bit line, bias node, source line, etc.). Tatsukawa's dummy transistor DG2 does not couple memory cells within the NAND string (i.e., memory cells MC11, MC12) to the source line SL1, and thus cannot be seen as a select device. Rather, only transistor SGS1 functions to couple the memory cells MC 11, MC 12 to the source line SL1 (see Appeal Brief page 4, paragraph 4 to page 5, paragraph 1).

In response to (I-b), Tatsukawa clearly discloses and shows DG2 is selectively activated by control signal SD2 applied to its gate; and therefore, DG2 is seen as a selection device.

Further, Examiner submits that claim 1 does not specifically recite any relationship to the functionality of the second selection devices with respect to the one NAND string. In other words, there is no specific relationship recited in claim 1 requiring the all of the second selection device are used to select the NAND string. Instead, claim 1 simply sets forth that the second series-selection devices are included at a second end of the NAND string. Thus, Examiner submits that Appellant's arguments art based upon limitations which are not recited in claim 1 in order to distinguish the claim over Tatsukawa.

However, assuming arguendo that this unrecited limitation is inherent in claim 1, which it is not, then Examiner submits the following to rebut Appellant's argument.

Appellant has presented his argument base on the assumption that the only function of a select device is coupling, in this case, between NAND string and source line. However, it is noted that the functions of a select device are not limited to an intermediate device for connecting between two elements. For example in Tatsukawa, DG2 is selected for the purpose of decrease the resistance between the sub-source line and the source line as disclosed in Tatsukawa, column 7 lines 29-49, where DG2 and DG4 are described in the context of different memory cell arrangement than FIG. 8, to wit:

> Sub-source line SSL1 is connected to a source line SL1 via source-side block select transistor SGS1 made conductive in response to source-side block select signal SS1. *This source line SL1 is connected to a source-side dummy transistor DG2 made conductive on in response to a drain-side block select signal SG2.* One conduction node (drain) of dummy transistor DG2 is set to the open state.
>
> Sub-bit line SBL2 is electrically coupled to a node NDb on main bit line MBL via a drain-side dummy transistor DG3 receiving source-side block select signal SS1 on its

> gate and a drain-side block select transistor SGD2 receiving drain-side block select signal SD2 on its gate.
>
> Sub-source line SSL2 is connected to a source line SL2 via source-side block select transistor SGS2 made conductive in response to source-side block select signal SS2. *This source line SL2 is connected to a source-side dummy transistor DG4 receiving a drain-side block select signal SG1 on its gate.* One conduction node (drain) of dummy transistor DG4 is set to the open state. *With no channel resistance of the dummy transistor, a resistance between the sub-source line and the source line can be small.* (Emphasis added)

Tatsukawa still discloses and shows DG2 is selectively activated; and therefore, DG2 is seen as a selection device.

(I-c) Appellant argues that dummy transistor DG2 *cannot be seen as a select device* because any extraneous transistor structure formed "beyond" the connection to the memory array node in question cannot be part of the NAND string. In this case, the extraneous dummy transistor DG2 is connected to the same source line SL1, but is not part of the NAND string, does not function to select the NAND string, and cannot be seen as being a select device (see Appeal Brief page 5, paragraph 2).

In response to (I-c), Tatsukawa clearly discloses and shows DG2 is selectively activated by control signal SD2 applied to its gate; and therefore, DG2 is seen as a selection device.

Further, Examiner submits that claim 1 does not specifically recite any relationship to the functionality of the second selection devices with respect to the NAND string. In other words, there is no specific relationship recited in claim 1 requiring the second selection devices are used to select the NAND string. Instead, claim 1 simply sets forth that the "NAND string includes second... series selection devices... at a second end." Thus, Examiner submits that Appellant's

arguments art based upon limitations which are not recited in claim 1 in order to distinguish the claim over Tatsukawa.

However, assuming arguendo that this unrecited limitation is inherent in claim 1, which it is not, then Examiner submits the following to rebut Appellant's argument.

Please see above response to argument (I-b).

(I-d) Appellant argues that the dummy transistor DG2 is made conductive in response to a block select signal SD2. When active, this signal SD2 is actually selecting the *other* sub-bit line SBL2 and coupling it to the major bit line MBL, *not* the sub-bit line SBL1. Examiner's statement "Dummy transistor DG2 turns on/off in response to drain-side block *select signal* SD2, therefore it is seen as a selection device" is total misunderstanding or ignoring the issue of *which* sub-source line or sub-bit line is being selected, in addition to the fundamental question that such dummy transistor cannot actually participate in *selecting* any of such lines, since its drain terminal is open! It cannot couple a sub-source line to the source line, nor can it couple a sub-bit line to the major bit line. It simply *cannot select anything* and couple it to the source line (see Appeal Brief page 5, paragraph 7 to page 6, paragraph 1).

In response to (I-d), Tatsukawa clearly discloses and shows DG2 is selectively activated by control signal SD2 applied to its gate; and therefore, DG2 is seen as a selection device.

Further, Examiner submits that claim 1 does not specifically recite any relationship to the functionality of the second selection devices with respect to the NAND string. In other words, there is no specific relationship recited in claim 1 requiring the second selection devices are used

to select the NAND string. Instead, claim 1 simply sets forth that the "NAND string includes second... series selection devices... at a second end." Thus, Examiner submits that Appellant's arguments art based upon limitations which are not recited in claim 1 in order to distinguish the claim over Tatsukawa.

However, assuming arguendo that this unrecited limitation is inherent in claim 1, which it is not, then Examiner submits the following to rebut Appellant's argument.

Appellant has presented argument based on the assumption that the only function of a select device is coupling the NAND string to the source line. Tatsukawa show that in response to block select signal SD2, transistor SGD2 turns on to couple sub-bit line SBL2 to main bit line MBL, and dummy transistor DG2 turns on to decrease the resistance between the sub-source line and the source line SL1. In short, dummy transistor DG2 is selectively "turned on," or activated, by control signal SD2 applied to its gate, and for at least this specific reason, DG2 is seen as a select device.

(I-e) Appellant further argues that Tatsukawa is trying to point out, in column 7, lines 41-49, describing FIG. 1, that the resistance that couples the sub-source line SSL2 to the source line SL2 results only from the one select transistor SGS2 (i.e., when conductive). This transistor is the only device that actually couples the sub-source line SSL2 to the source line SL2, and is the only transistor that can properly be viewed as a select device at this end of the NAND string. In other words, Appellant argues that dummy transistor DG4 does not belong to the NAND string and cannot be seen as a select device (see Appeal Brief page 6, paragraph 3).

In response to (I-e), Tatsukawa clearly discloses and shows DG4 is selectively activated by control signal SD1 applied to its gate (see Fig. 8); and therefore, DG4 is seen as a selection device.

Further, Examiner submits that claim 1 does not specifically recite any relationship to the functionality of the second selection devices with respect to the NAND string. In other words, there is no specific relationship recited in claim 1 requiring the second selection devices are used to select the NAND string. Instead, claim 1 simply sets forth that the "NAND string includes second... series selection devices... at a second end." Thus, Examiner submits that Appellant's arguments art based upon limitations which are not recited in claim 1 in order to distinguish the claim over Tatsukawa.

However, assuming arguendo that this unrecited limitation is inherent in claim 1, which it is not, then Examiner submits the following to rebut Appellant's argument.

See above response to argument (I-a) where Appellant argues that dummy transistor DG2 does not correspond to a select device for the NAND string, and response to argument (I-b) where Appellant argues that dummy transistor DG2 cannot be seen as a select device. Dummy transistor DG4 operates similar to DG2 and the response to (I-a) and (I-b) is similarly applicable. In short, dummy transistor DG4 is selectively "turned on," or activated, by control signal SD1 applied to its gate, and for at least this specific reason, DG4 is seen as a select device.

(I-f) Appellant argues, "Tatsukawa nowhere states that the dummy transistor DG2 is selected for equalizing electrical characteristics" (see Appeal Brief page 7, paragraph 2).

In response to (I-f), this argument has no bearing on any claimed subject matter; and thus, Examiner submits that Appellant's arguments art based upon limitations which are not recited in claim 1 in order to distinguish the claim over Tatsukawa.

Tatsukawa still discloses and shows DG2 is selectively activated by control signal SD1 connected to its gate (see Fig. 8); and therefore, DG2 is seen as a selection device.

(I-g) Appellant argues that Examiner's argument "the claim language, especially claim 1, merely calls for first and second groups of control signals, *not the selection devices*, to couple a series connected string of memory cell within the NAND string to the global array line and bias node" reads key limitations entirely out of the claim, for claim 1 also recites:

> ... said NAND strings *including* at a first *end thereof* a respective *plurality* of series selection devices of like type, wherein each NAND string includes a second *plurality* of series selection devices of like type at a second *end thereof*... [emphasis added]

These are structural limitations that cannot be properly ignored, but that is precisely what the Examiner's argument does. Applicant submits that Tatsukawa fails to disclose each limitation of claim 1, and that the Examiner has therefore not established a prima facie case for anticipation.

In response to (I-g), Examiner submits that claim 1 does not specifically recite any relationship between the first/second selection devices and the first/second group of control signals. In other words, there is no specific relationship recited in claim 1 requiring the first/second selection devices are controlled by the first/second group of control signals. Instead, claim 1 simply sets forth "a respective plurality of series selection devices," "a second plurality

of series selection devices," "a first group of control signals," and "a second group of control signals," with no specific functional dependencies. Thus, Examiner submits that Appellant's arguments art based upon limitations which are not recited in claim 1 in order to distinguish the claim over Tatsukawa.

Examiner maintains her argument that claim language of claim 1 calls for first and second groups of control signals, *not the selection devices*, to couple a series connected string of memory cell within the NAND string to the global array line and bias node. The claim recites no physical connection between the "plurality of series connection devices" mentioned in the preamble, and the first and second "groups of control signals" mentioned in the body of the claim. Therefore, there is no structural limitation which links the plurality of series connection devices to the groups of control signals as Appellant argues in his response. The Examiner did not ignore this alleged structural limitation, as Appellant argues, since this limitation is not stated in the claim. In response to Appellant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the plurality of select devices couple one end of the NAND string to a bias node) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Ground II: The rejection of claims 27-28 under 35 U.S.C. 103(a) as being unpatentable over Tatsukawa in view of U.S. Patent No. 6,411,548 to Sakui et al. (hereinafter "Sakui").

Claims 27-28

(II-a) Appellant argues that Tatsukawa fails to disclose each limitation of claim 1 and that Sakui does not cure such presumed deficiencies Tatsukawa has regarding claim 1.

In response to (II-a), Appellant has not shown that Tatsukawa and Sakui are improperly combined. Rather, Appellant urges that claims 27 and 28 are patentable for the reason that they depend from a presumed patentable claim 1. Examiner submits that Tatsukawa anticipates all limitations set forth in claim 1.

Dependent claim 27 further recites "series selection devices having a charge storage dielectric." One of ordinary skill in the art at the time of the invention would most certainly understand that the series selection device of Tatsukawa inherently, or implicitly, has a charge storage dielectric. Examiner, however, submits that Sakui strictly show series selection devices having a charge storage dielectric (see Fig. 44) and both Sakui and Tatsukawa are combinable for the undisputed motivation(s) set forth in the rejection of claim 27.

Dependent claim 28 further recites "series selection devices... are maintained by periodic programming biasing to a higher threshold voltage than fabricated." One of ordinary skill in the art at the time of the invention would most certainly understand that the series selection device of Tatsukawa inherently, or implicitly, are maintained by periodic programming biasing to a higher threshold voltage than fabricated. Examiner, however, submits that Sakui further show series selection devices are maintained by periodic programming biasing to a higher threshold voltage than fabricated (see Fig. 52, 53) and both Sakui and Tatsukawa are combinable for the undisputed motivation(s) set forth in the rejection of claim 27.

Therefore, the rejection of claims 27-28 over Tatsukawa in view of Sakui is considered proper and is maintained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

VanThu Nguyen

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